O I P E JC48
JAN 1 6 2004
PATENT & TRADEMARK OFFICE

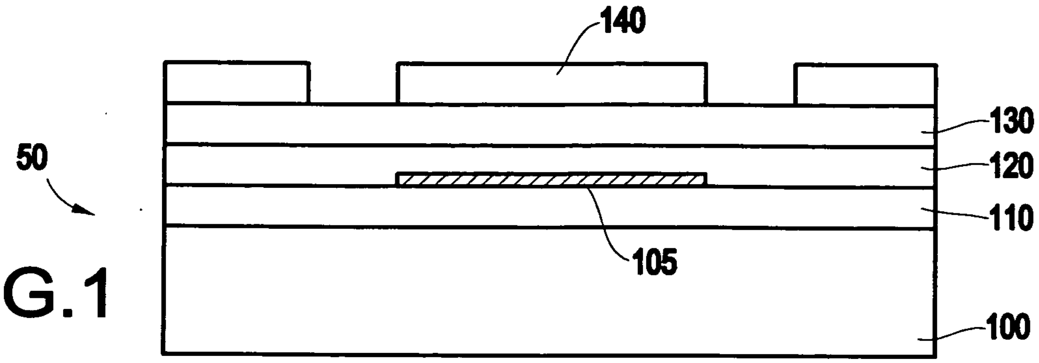

FIG.1

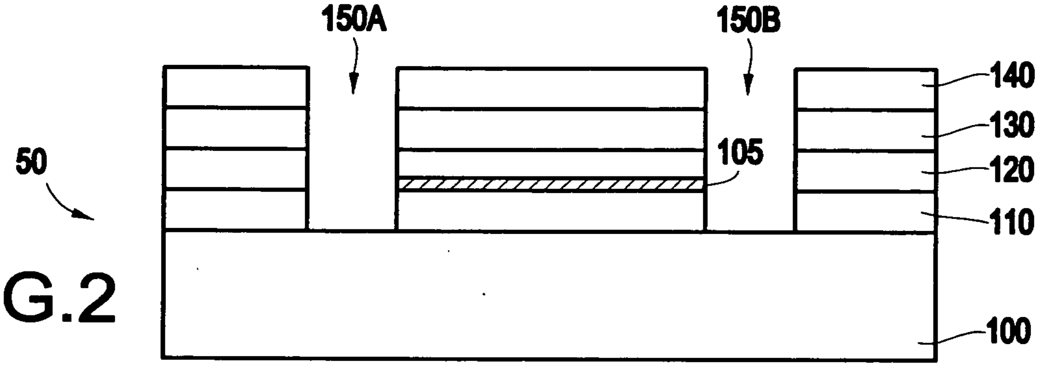

FIG.2

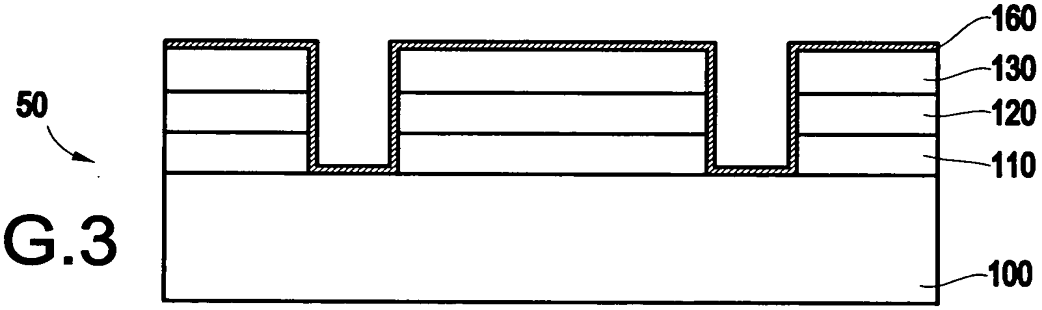

FIG.3

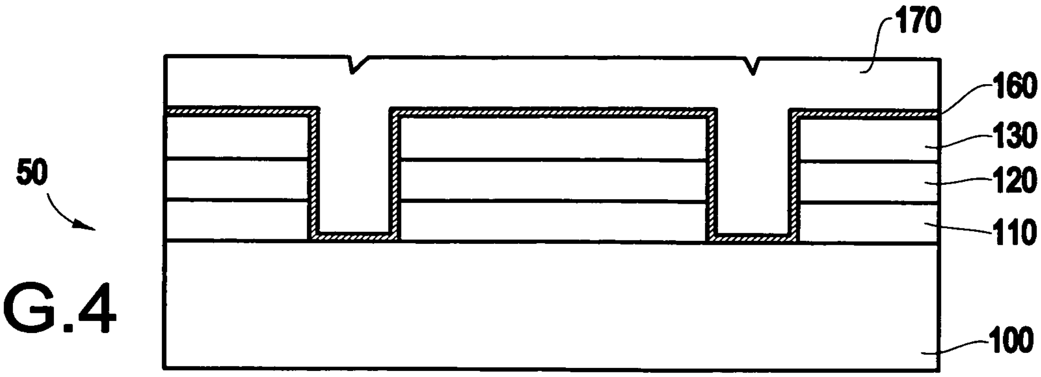

FIG.4

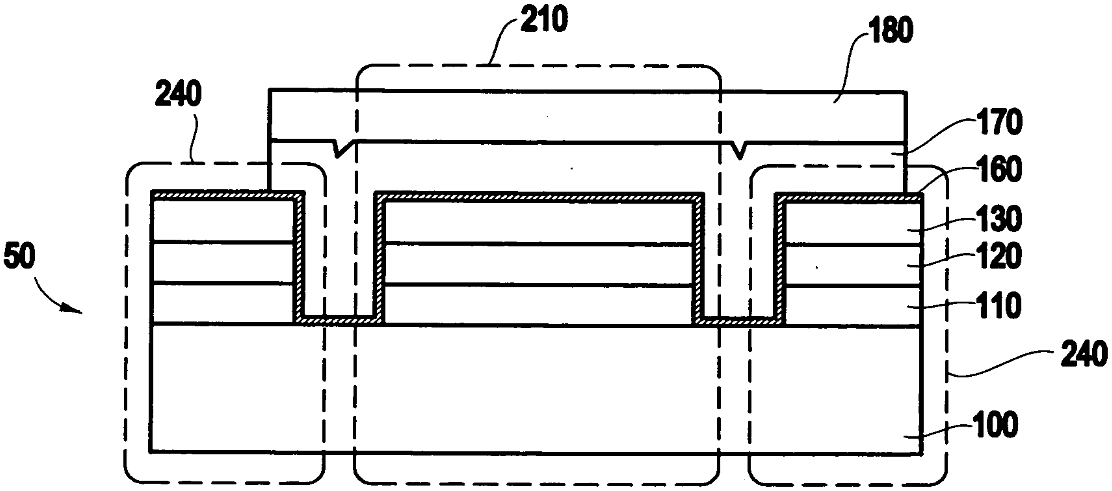

FIG.5A

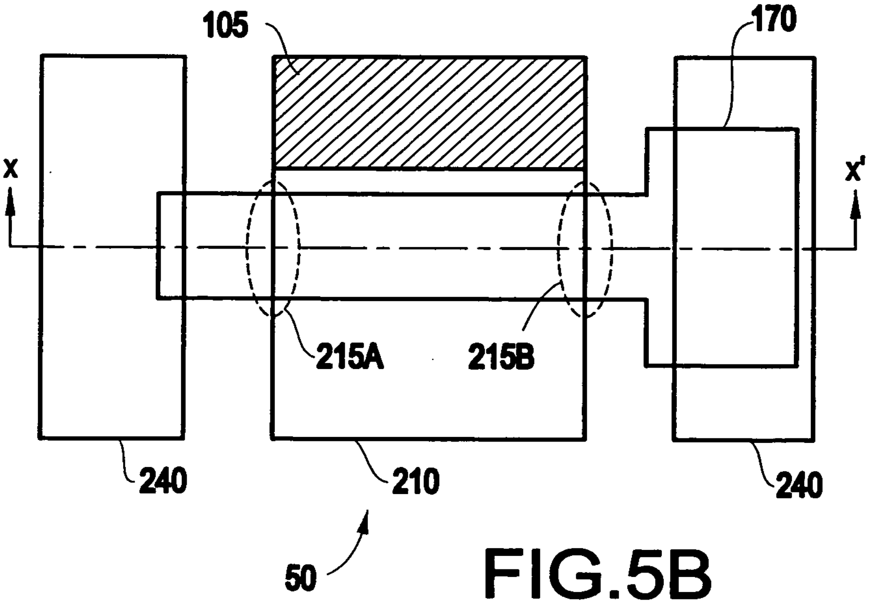
x
x'

FIG.5B

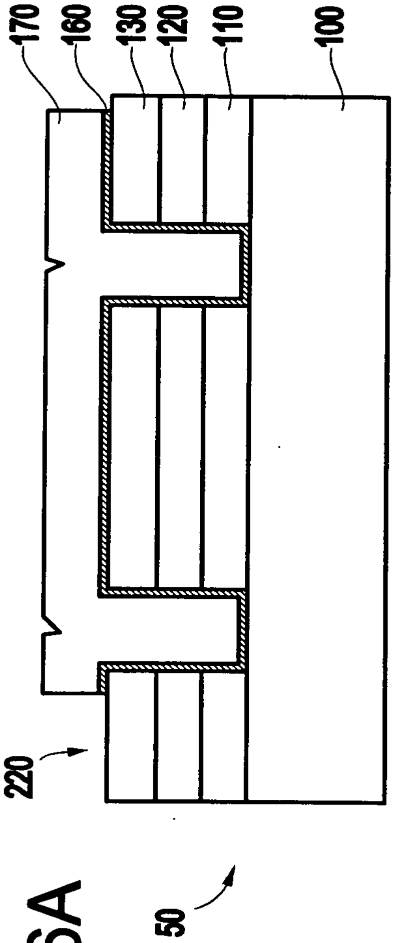

FIG.6A

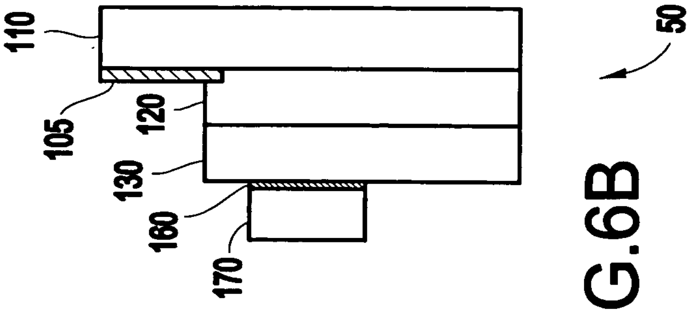

FIG.6B

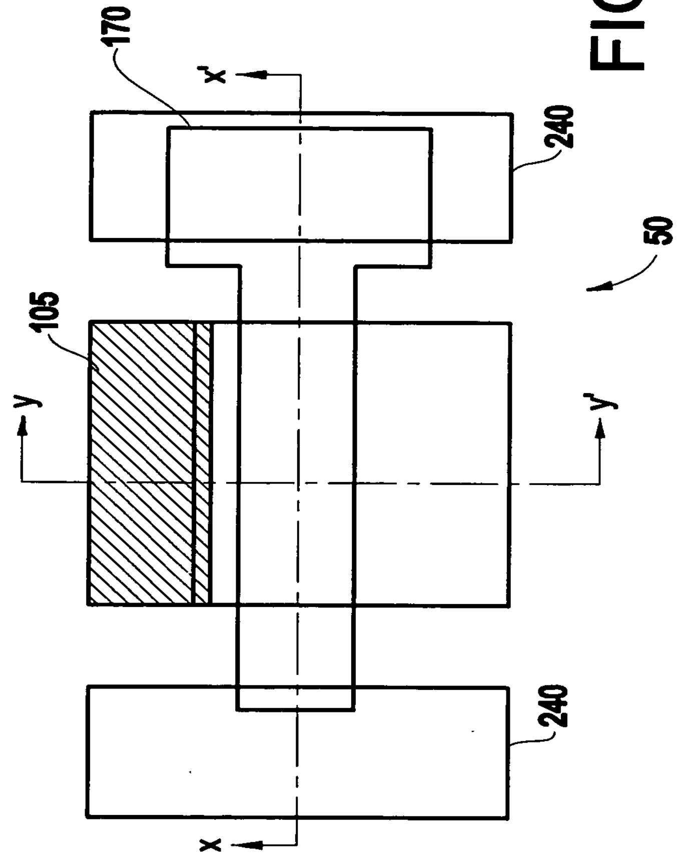

FIG.6C

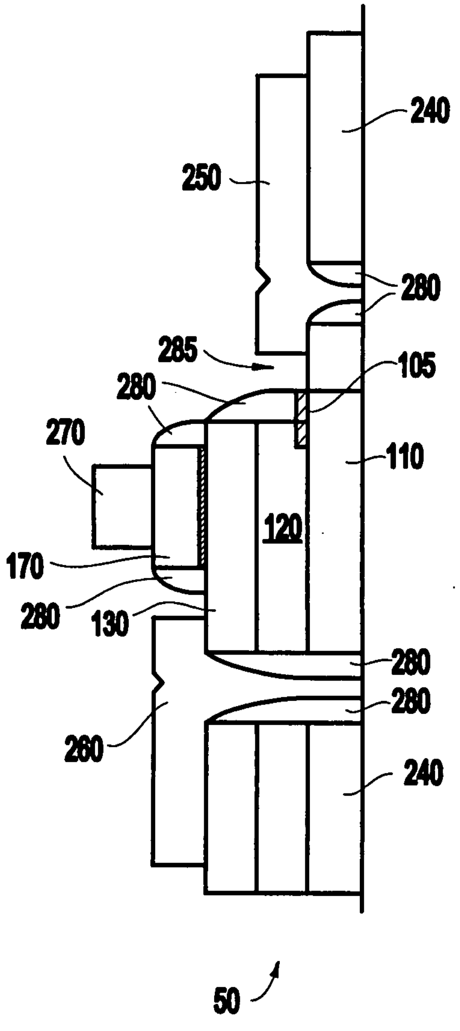

FIG.7A

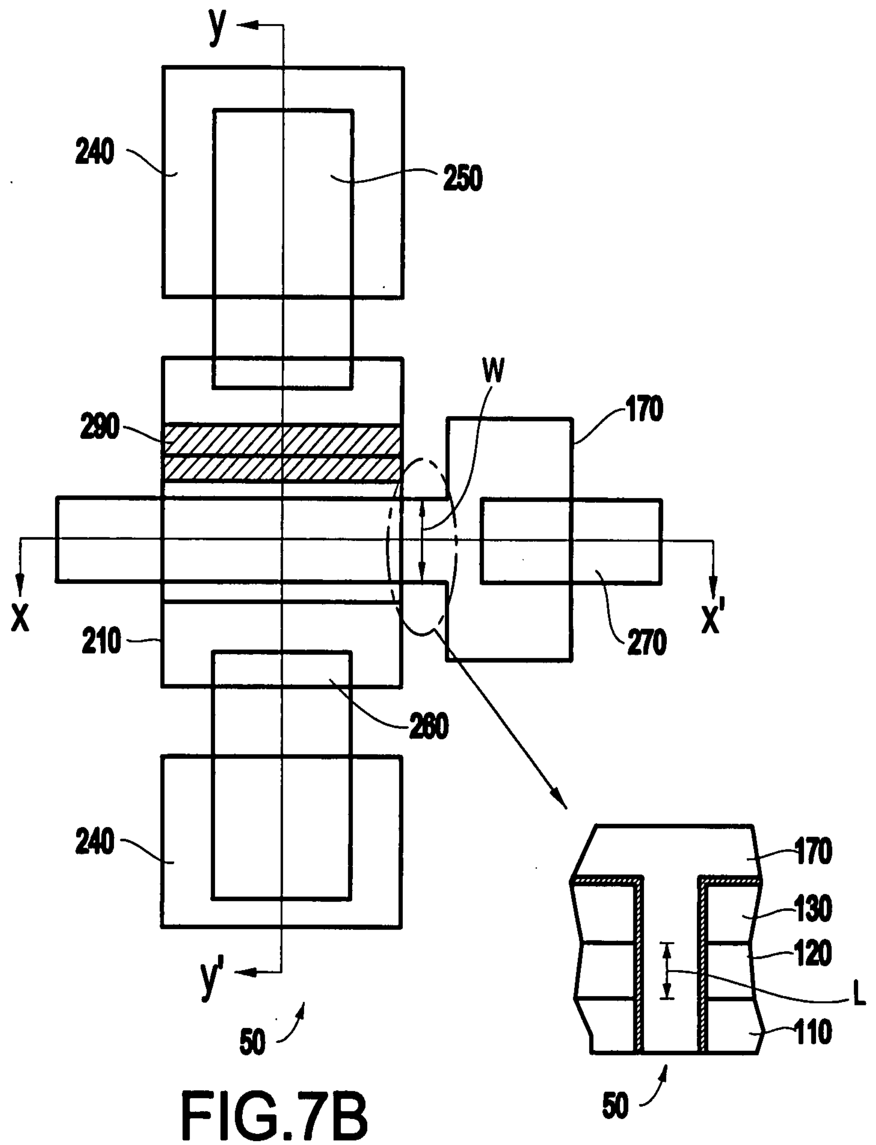

FIG.7B

FIG.7C

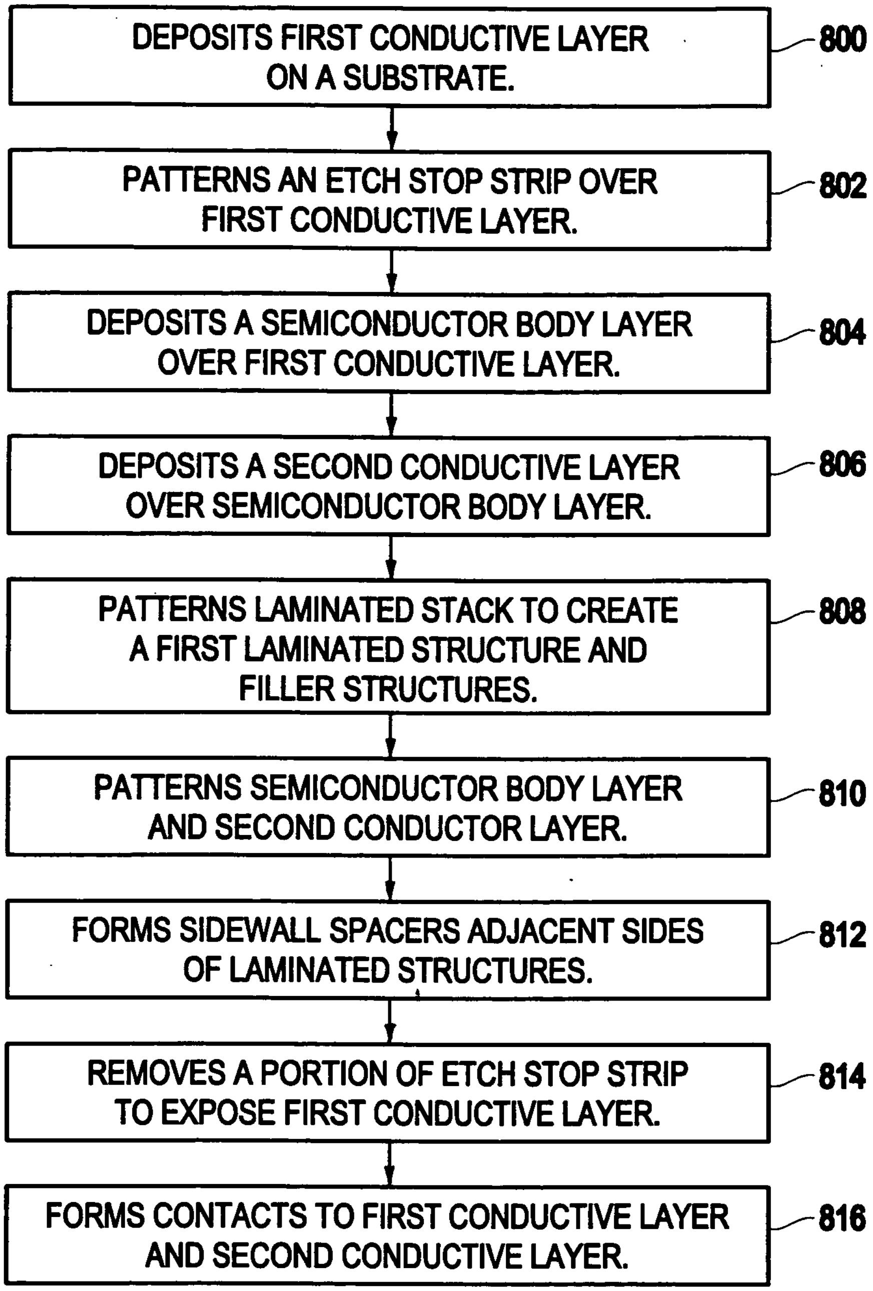
DEPOSITS FIRST CONDUCTIVE LAYER ON A SUBSTRATE.
800
PATTERNS AN ETCH STOP STRIP OVER FIRST CONDUCTIVE LAYER.
802
DEPOSITS A SEMICONDUCTOR BODY LAYER OVER FIRST CONDUCTIVE LAYER.
804
DEPOSITS A SECOND CONDUCTIVE LAYER OVER SEMICONDUCTOR BODY LAYER.
806
PATTERNS LAMINATED STACK TO CREATE A FIRST LAMINATED STRUCTURE AND FILLER STRUCTURES.
808
PATTERNS SEMICONDUCTOR BODY LAYER AND SECOND CONDUCTOR LAYER.
810
FORMS SIDEWALL SPACERS ADJACENT SIDES OF LAMINATED STRUCTURES.
812
REMOVES A PORTION OF ETCH STOP STRIP TO EXPOSE FIRST CONDUCTIVE LAYER.
814
FORMS CONTACTS TO FIRST CONDUCTIVE LAYER AND SECOND CONDUCTIVE LAYER.
816

FIG.8

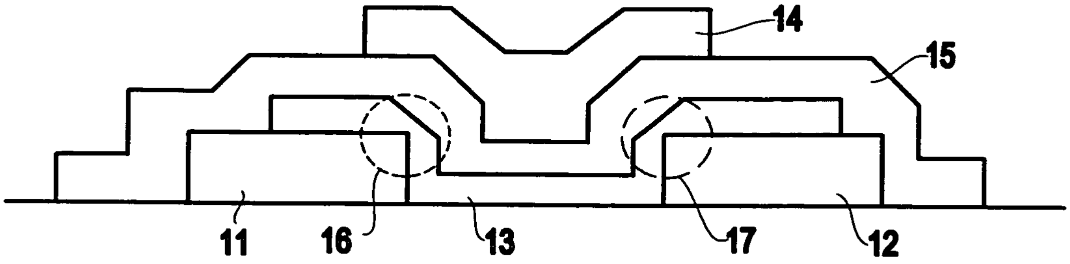

FIG.9A

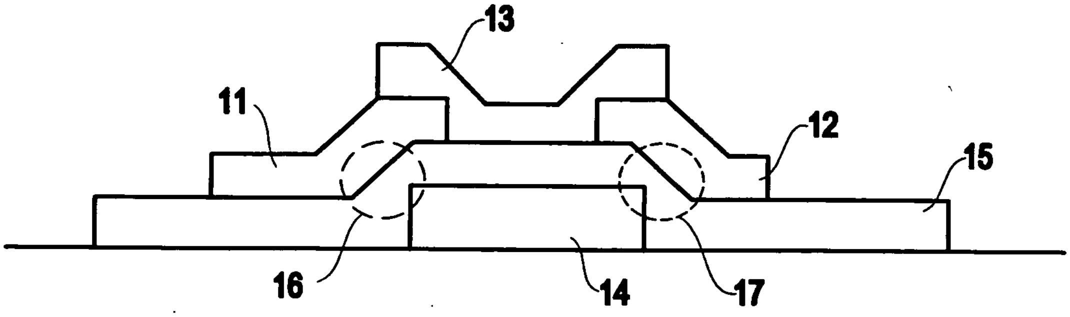

FIG.9B